USE OF STATE TRAJECTORY PREDICTION IN HYSTERESIS CONTROL FOR ACHIEVING FAST TRANSIENT RESPONSE OF THE BUCK CONVERTER

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Abstract - **A dynamic hysteresis control of the buck converter for achieving high slew-rate response to disturbances is proposed. The hysteresis band is derived from the output capacitor current that predicts the output voltage magnitude after a hypothesized switching action. Four switching criteria are formulated to dictate the state of the main switch. The output voltage can revert to the steady state in two switching actions after a large-signal disturbance. The technique is verified with the experimental results of a 50W buck converter.**

I. INTRODUCTION

Recent advancements in high-speed microprocessor and digital signal processor technologies have drastically increased the significance of large-signal dynamics in dc/dc power conversion. Linear regulators are considered to be a good choice for dealing with fast dynamic response, but they are counteracted by poor efficiency and are impractical in high-current applications. Switching regulators can improve efficiency, but they exhibit slow dynamic response. Circuit designers generally focus on researching either the power circuit or the controller to achieve fast transient response.

Among various choices, conventional buck and synchronous rectifier buck converters are the most popular power conversion stage in applications, like voltage regulator module (VRM), requiring fast transients. A simple way of improving transient response is to reduce the output filter inductor value and increase the output filter capacitance and decoupling capacitance. However, this will cause large inductor current ripple, resulting in high conduction and switching losses, and core loss in the inductor. In addition, due to the space constraint, increasing the capacitance is an impractical approach. Much research effort has been paid on developing new converter configurations, such as multiphase interleaved topology and its enhancement with coupling inductors, and stepping inductor topology. Apart from converter topologies, other research focus on the control schemes to improve the large-signal dynamics in dc/dc conversion. Concept of current control [1, 2] combines the slow-varying voltage loop with the fast-varying current loop to dictate the state of the main switch. A best performance can be obtained when the current reference and the inductor current are closely related [3]. V^2 control provides fast loop responses comparable to a linear regulator [4, 5]. However, the equivalent series resistance of the output capacitor is a critical factor that considerably affects the converter performance. Another one is the hysteresis control [6]-[8] that the controller turns the switch on when the output is below the hysteresis band, and vice versa. However, during the startup and load disturbance, the energy stored in the inductor will continuously boost the output, even if the controller turns the main switch off. Eventually, the settling time will be lengthened. This paper proposes a state trajectory prediction (STP) technique to enhance the transient response of the buck converter with hysteresis control. The output can revert to the steady state in two switching actions after a large-signal disturbance. The theoretical predictions have been verified experimentally.

II. PRINCIPLES OF OPERATION

Fig. 1 shows the circuit schematic of the buck converter.

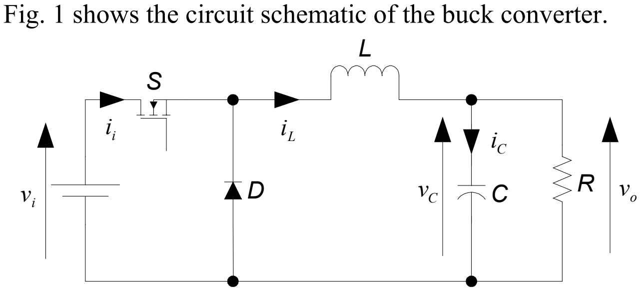


Fig. 1 Buck converter.

When the switch S is on,

$$\frac{d\,i_L}{d\,t} = \frac{1}{L}(v_i - v_o) \text{ and } \frac{d\,v_o}{d\,t} = \frac{d\,v_C}{d\,t} = \frac{1}{C} i_C \tag{1}$$

When S is off and D is on,

$$\frac{d\,i_L}{d\,t} = -\frac{1}{L} v_o \text{ and } \frac{d\,v_o}{d\,t} = \frac{d\,v_C}{d\,t} = \frac{1}{C} i_C \tag{2}$$

When S and D are off,

$$\frac{d\,i_L}{d\,t} = 0 \text{ and } \frac{d\,v_o}{d\,t} = \frac{d\,v_C}{d\,t} = \frac{1}{C} i_C \tag{3}$$

If the output ripple voltage is much smaller than the average output voltage at the steady state, the output current i_o is relatively constant. Since $i_L = i_C + i_o$, the change of i_L, Δi_L, equals the change of i_C, Δi_C. Fig. 2 shows the typical waveforms of v_o and i_C. v_o varies between a maximum value of $v_{o,\max}$ and a minimum value of $v_{o,\min}$. The state of *S* is determined by predicting the area under i_C with a hypothesized switching action till $i_C = 0$ and comparing the area with a fixed ratio of the output error at that instant.

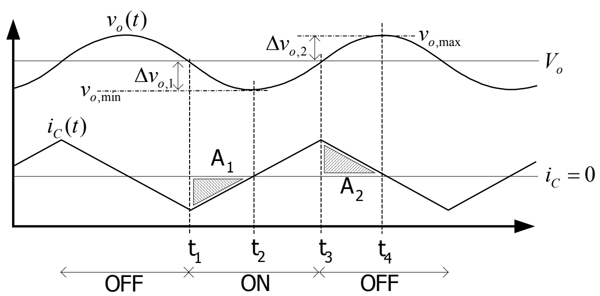


Fig. 2 Typical waveforms of v_o and i_c.

1) Criteria for switching on S

As shown in Fig. 2, *S* is originally in the off state and is switched on at the hypothesized time instant t_1. The objective is to determine t_1, so that v_o will be equal to $v_{o,\min}$ at t_2 (at which $i_C = 0$). The shaded area A_1 under i_C is integrated from t_1 to t_2. Thus,

$$\Delta v_{o,1} = v_o(t_1) - v_{o,\min} = -\frac{1}{C}\int_{t_1}^{t_2} i_C \, dt \tag{4}$$

If A_1 is approximated by a triangle, it can be shown that

$$\int_{t_1}^{t_2} i_C \, dt \cong -\frac{1}{2}\frac{L\, i_C^{\,2}(t_1)}{[v_i(t_1) - v_o(t_1)]} \tag{5}$$

In order to ensure that v_o will not go below $v_{o,\min}$, *S* should be switched on when

$$\begin{aligned} v_o(t_1) &\le v_{o,\min} + \frac{1}{2}\frac{L\, i_C^{\,2}(t_1)}{C\,[v_i(t_1) - v_o(t_1)]} \\ &= v_{o,\min} + K_1(v_i, v_o)\, i_C^{\,2}(t_1) \end{aligned} \tag{6}$$

and

$$i_C(t_1) < 0 \tag{7}$$

2) Criteria for switching off S

As shown in Fig. 2, *S* is originally in the on state and is switched off at the hypothesized time instant t_3. The objective is to determine t_3, so that v_o will be equal to $v_{o,\max}$ at t_4 (at which $i_C = 0$). The shaded area A_2 under i_C is integrated from t_3 to t_4. Thus,

$$\Delta v_{o,2} = v_{o,\max} - v_o(t_3) = \frac{1}{C}\int_{t_3}^{t_4} i_C \, dt \tag{8}$$

Again, A_2 is approximated by a triangle. It can be shown that

$$\int_{t_3}^{t_4} i_C \, dt \cong \frac{1}{2}\frac{L\, i_C^{\,2}(t_3)}{v_o(t_3)} \tag{9}$$

In order to ensure that v_o will not go above $v_{o,\max}$, *S* should be switched off when

$$\begin{aligned} v_o(t_3) &\ge v_{o,\max} - \frac{1}{2}\frac{L\, i_C^{\,2}(t_3)}{C\, v_o(t_3)} \\ &= v_{o,\max} - K_2(v_o)\, i_C^{\,2}(t_3) \end{aligned} \tag{10}$$

and

$$i_C(t_3) > 0 \tag{11}$$

If K_1 and K_2 are zero, the control is same as an ordinary hysteresis control. The time-varying error terms in (6) and (10) (i.e., the second term) affect the output ripple and improve the transient responses, as compared with the ordinary hysteresis control. For the sake of simplicity, v_i and v_o in (6) and (10) are taken to be their nominal values. Thus K_1 and K_2 are constants. The criteria of (6), (7), (10), and (11) are applied for both steady state operations and large-signal disturbances. Fig. 3 shows the block diagram of the control.

III. EXPERIMENTAL VERIFICATIONS

A 50W 24V/5V prototype has been built. The component values are: L = 100μH, C = 470 μF, $v_{o,\min}$ = 4.975V, and $v_{o,\max}$ = 5.025V. v_o is regulated at 5V. The theoretical state-plane trajectories operating at the rated load under five different load disturbances without and with the STP are shown in Figs. 4(a) and 4(b), respectively.

They show the changes of i_L (i.e., $\hat{i}_L$) and v_o (i.e., $\hat{v}_o$) during the transient period. The origin (0, 0) represents the steady-state operating point of v_o = 5V and i_L = 10A. The initial deviations from the steady state operating point (i.e., the testing conditions) are labeled from ‘1’ to ‘5’ in the figures. The initial inductor currents prior load changes [i.e., $i_L(0^-)$], the settling time, the percentage output overshoots are tabulated in Table I. The settling time is defined as the time taken that v_o falls into ±1% tolerance bands - the dash lines shown in the figures. It can be seen that the transient performances are improved with the STP, particularly when the output load is increased.

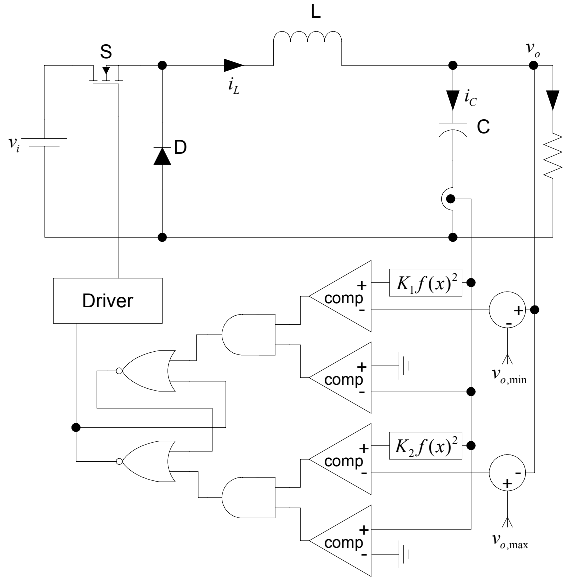
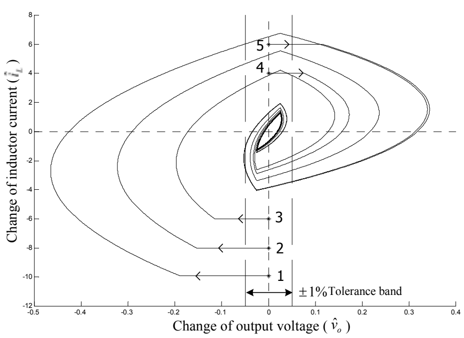
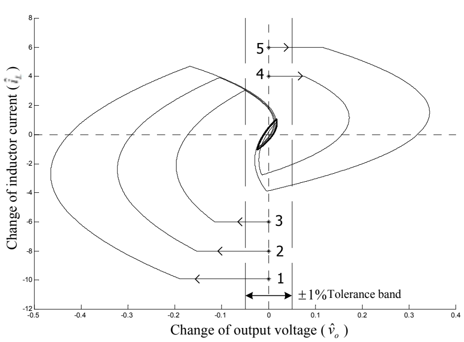


Fig. 3 Block diagram of the control technique.



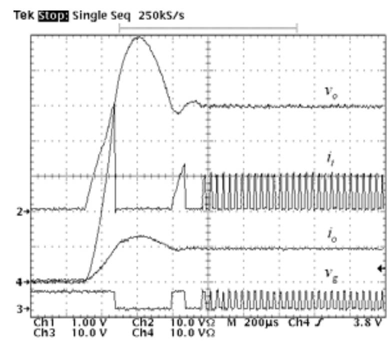
(a) Without STP.



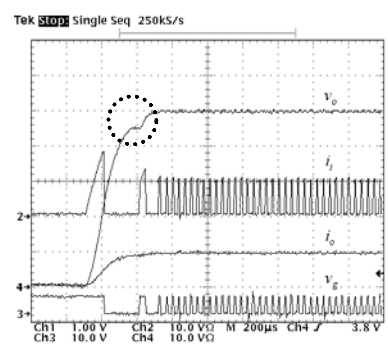
(b) With STP.

Fig. 4 Theoretical state-plane trajectories of the buck converter operating at the rated power from different initial conditions.

Fig. 5 shows the startup transients of v_o, the input current i_i, i_o, and the gate drive signal v_g without and with the STP. The settling time of the output transient without STP is 650μs, whilst the one with STP is 350μs. As expected, the ordinary hysteresis control turns off the main switch when v_o is higher than the hysteresis band. The stored energy in the inductor will further boost the output after the main switch is off. The output overshoot and settling time are thus increased. The output profile is much improved with the STP. However, as i_o is not in the steady state during the startup, Δi_L is different from Δi_C. There are discrepancies in predicting the output. As circled in Fig. 5(b), two extra switching actions are introduced, but it does not affect the overall performance.



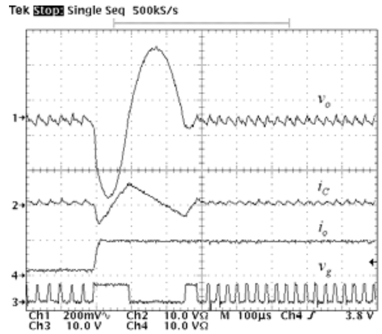
(a) Without STP.



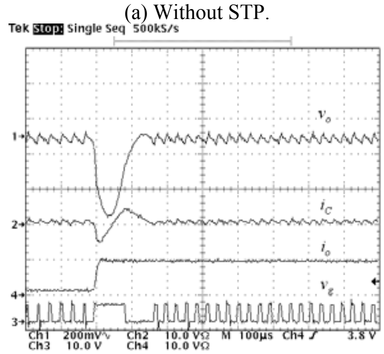
(b) With STP.

Fig. 5 Startup transients. [v_o: output voltage (1V/div), i_i : input current(10A/div), i_o : load current (10A/div), v_g : gate drive signal(10V/div)].

Fig. 6 shows the waveforms when i_o is increased suddenly from 1A (5W) to 10A (50W). The settling time of the transients without STP is 240μs and the one with STP is about 100μs. The main switch with STP is switched off earlier than the one without STP, since v_o is predicted *apriori* before switching off the main switch. The output can revert to the steady state in two switching actions. Thus, the STP can effectively enhance the transient response of the buck converter using hysteresis control without significant modification of the control.



(a) Without STP.



(b) With STP.

Fig. 6 Transient responses when i_o is changed from 1A (5W) to 10A (50W). [v_o : output voltage (200mV/div), i_C: capacitor current(10A/div), i_o: load current (10A/div), v_g: gate drive signal(10V/div)]

IV. Conclusions

An STP technique that is applied to the hysteresis control has been proposed. It can enhance the transient response of the buck converter. The output voltage can revert to steady state within two switching actions when it is subject to large-signal disturbances. The STP performances have been verified with experimental measurements. Further research will be dedicated to study the sensitivities of the component values on affecting the performances.

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TABLE I Comparisons of the Converter Transient Responses Without and With the STP

Testing condition	1		2		3		4		5	
$i_L(0^-)$ (A)	0.1		2		4		14		16	
	Without STP	With STP	Without STP	With STP	Without STP	With STP	Without STP	With STP	Without STP	With STP
Settling time (µs)	248.7	102.4	182.7	79.3	135.4	53.3	77.0	77.0	144.1	118.1
% output overshoot	5.7	0.0	3.7	0.0	1.8	0.0	2.4	2.4	5.8	5.8
Max. inductor current (A)	16.8	14.7	15.5	13.9	14.2	13.0	14.0	14.0	16.0	16.0